8:30 Breakfast and Registration
8:50 Welcome
9:00 1st Invited Talk
   Rolf Drechsler, University of Bremen, Germany
   Coverage at the Formal Specification Level
10:00 Coffee Break
10:30 System
   • Alberto Griggio and Marco Roveri, Comparing Different Variants of the IC3 Algorithm for
     Hardware Model Checking
   • Paolo Camurati, Carmelo Loiacono, Paolo Pasini, Denis Patti and Stefano Quer, To split or
     to group: from divide-and-conquer to sub-task sharing in verifying multiple properties
   • Bardh Hoxha, Hoang Bach, Houssam Abbas, Adel Dokhanchi, Yoshihiro Kobayashi and
     Georgios Fainekos, Towards Formal Specification Visualization for Testing and Monitoring
     of Cyber-Physical Systems
12:00 Tools I
   • Sebastiaan Joosten, Freek Verbeek and Julien Schmaltz, WickedXmas: Designing and
     Verifying on-chip Communication Fabrics
12:30 Lunch
13:30 2nd Invited Talk
   Wolfgang Kunz, University of Kaiserslautern, Germany
   The big hurdles for FV tools in industrial practice – can we overcome them in system-level
   design flows?
14:20 Tools II
   • Daryl Stewart, David Gilday, Daniel Nevill and Thomas Roberts, Processor Memory System
     Verification using DOGReL: a language for specifying End-to-End properties
   • Tayfun Gezgin, Raphael Weber and Markus Oertel, Multi-aspect Virtual Integration
     approach for Real-Time and Safety Properties
15:20 3rd Invited Talk
   Fahim Rahim, Atrenta Europe, Grenoble, France
   Efficiently using formal verification techniques to reduce power
16:00 Coffee Break
16:15 MEMOCODE final Key Note by Joseph Sifakis
   A framework for modeling architectures and their properties

(DIFTS attendees are invited to attend the MEMOCODE talk)